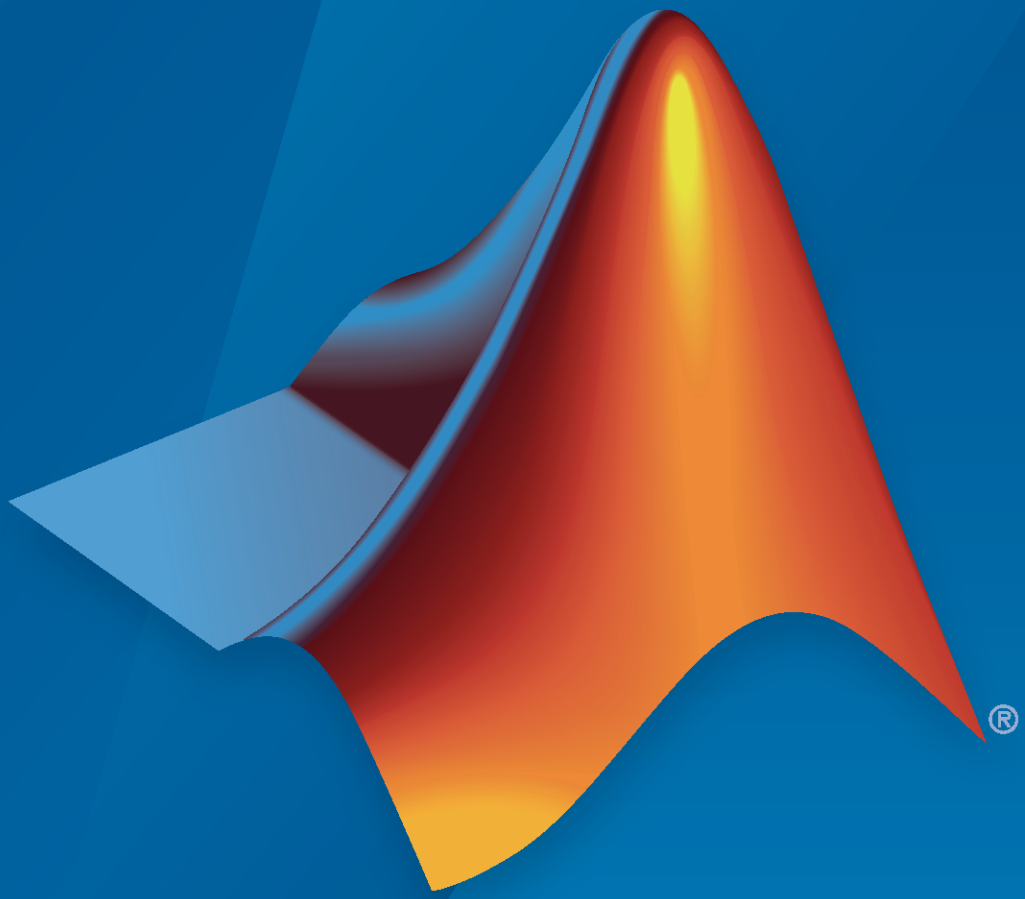
Signal Integrity Toolbox™ Release Notes



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Signal Integrity Toolbox™ Release Notes

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R2023a

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R2023a

Version: 1.3

New Features

Bug Fixes

Integration Between Apps and Command Window: Use MATLAB scripts to read data from app

You can now use MATLAB® scrips to execute commands to read the simulation data from the **Serial Link Designer** and **Parallel Link Designer** apps. For more information, see “Access Project Data from MATLAB Command Window”.

Updated Transmission Line Models in IsSpice4: Choose between RLGC or table-driven model

You can choose to implement an RLGC model or a table-driven model for a lossy multi-conductor transmission line in IsSpice4. For more information, see “Model Lossy Transmission Lines in Serial Link Designer” or “Model Lossy Transmission Lines in Parallel Link Designer”.

R2022b

Version: 1.2

Bug Fixes

PAMn Support: Select modulation and mapping when simulating with PAMn models

Both **Serial Link Designer** and **Parallel Link Designer** apps allow you to use PAMn levels up to 32 and support multiple mappings needed when simulating with PAMn models.

Eye Mask Rules Support: Use different rules in Parallel Link Designer and Serial Link Designer

You can now use the `Max Width Margin Mask` rule and the `Clocked Mask` rule to **Parallel Link Designer** STAT mode sheets.

You can now use the `Max Width Margin Mask` rule to **Serial Link Designer** sheets.

R2022a

Version: 1.1

Bug Fixes

DDR5 Clock Forwarding Example: Implement clock forwarding in DDR5

The DDR5 IBIS-AMI with Clock Forwarding example shows how to implement DDR5 in Memory-Down form factor with the IBIS-AMI feature Clock-Forwarding enabled for analysis of system margins for Clock vs. Address/Command and Strobe(DQS) vs. Data(DQ).

R2021b

Version: 1.0

New Features

Introducing Signal Integrity Toolbox: Design and analyze high speed serial and parallel links

Signal Integrity Toolbox™ provides a set of analysis tools and apps to configure, design, and analyze high speed serial and parallel links. You can generate experiments covering multiple parameters, extract design metrics, and visualize waveforms and results. You can also predict operating margins and link performance by analyzing transmitter, receiver, and channel interactions

Serial Link Designer App: Design and analyze high speed serial links

Use the **Serial Link Designer** app for end-to-end analysis of multi-gigabit serial links. Use IBIS-AMI models, PCB traces, vias, and connectors to analyze loss, reflections, crosstalk and more.

Parallel Link Designer App: Design and analyze high speed parallel links

Use the **Parallel Link Designer** app to determine setup/hold timing and voltage margins for high-speed parallel links. Use IBIS-AMI models, PCB traces, vias, and connectors to analyze parallel interfaces for compliance with timing and signal integrity constraints, reflections, crosstalk and more.

Signal Integrity Viewer App: View the signal integrity results of serial and parallel link designs

Use the **SI Viewer** app to view the results of the simulations done in **Serial Link Designer** or **Parallel Link Designer** app.

Design Space Exploration: Sweep parameters to quickly determine design trade-offs

Perform design of experiments by sweeping parameters and channels to explore the effect different combinations of design parameters on the link design. Utilize the Parallel Computing Toolbox™ to speed up the large-scale analysis.

Post-layout Verification: Import PCB schematics for post-layout signal integrity verification.

Validate the waveform quality, timing and crosstalk for single and multi-board configurations of PCB layouts. You need a license to RF PCB Toolbox™ to run the post-layout verifications in full capacity.

Signal Integrity Kits for Industry Standards: Analyze and implement standard interfaces from prepackaged kits

Check serial and parallel links for compliance with industry standards by using one of over 40 available compliance kits such as PCIe, DDR, USB, and Ethernet. For more information, see Signal Integrity Kits for Industry Standards.